III. Amendments to the Claims

Claims 25-31 are pending in the present application. Claims 25-29 and 31 have been amended as set forth below. Claim 30 has been canceled. Claims 47-53 have been added. This listing and version of the claims replaces all prior listing and versions of the claims.

1-24. (canceled)

25. (currently amended) An integrated multiple vertical npn transistor ESD protection structure on a semiconductor substrate, functionally connected between an integrated circuit input or output pin and ground which will prevent electrostatic discharge damage to said integrated circuit comprising:[[;]]

a first semiconductor layer having a first conductivity dopant ~~dopent~~ type;

a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopant ~~dopent~~ concentration;

a third semiconductor layer having a second conductivity dopant ~~dopent~~ type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity dopant ~~dopent~~ type laterally spaced from said first regions, being electrically connected to said third semiconductor layer

having a top element making electrical contact to said second regions and said second semiconductor layer[[.]]; and

a plurality of third regions of said first semiconductor layer conductivity dopant ~~dopent~~ type laterally spaced and interposed between said second regions,

wherein said third regions form multiple emitter elements, said multiple emitter elements being electrically connected by a conductor element with "N" horizontal stripe conductor elements connected in a contiguous comb like manner by a vertical contact conductor element at one end of said horizontal stripe conductor elements.

26. (currently amended) The ESD protection structure of claim 25 whereby the plurality of first regions together with the associated connected first semiconductor layer are with n dopant ~~dopent~~ and form multiple collector elements of a bipolar transistor array in which the base elements ~~bases~~ are formed by said third semiconductor ~~conductivity~~ layer and associated said plurality of second regions of p dopant ~~dopent, and by which multiple emitter elements are formed by said plurality of laterally spaced third regions of n type dopent~~.

27. (currently amended) The ESD protection structure of claim 26 ~~25~~ whereby said plurality of laterally spaced ~~pluralities of~~ third ~~emitter~~ regions by which said multiple emitter elements are formed are arranged in an alternating array within said third semiconductor ~~base~~ layer, with "N" number of emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

28. (currently amended) The ESD protection structure of claim 27 ~~25~~ whereby said ~~first~~ collector elements ~~regions~~ have horizontal contact conductor stripes at the top and bottom of said transistor array which are ultimately connected together and to a first voltage source of said integrated circuit input or output ~~input/output~~ pin.

29. (currently amended) The ESD protection structure of claim 28 ~~25~~ whereby said base elements have horizontal conductor contact stripes, a first base horizontal conductor contact stripe positioned ~~array comprises a said contact and said emitter contact region, and a said second semiconductor base horizontal contact region~~ between the bottom horizontal collector contact stripe and said ~~a~~ "N" horizontal stripe conductor elements and a second base horizontal conductor contact stripe positioned between the top horizontal collector contact stripe and said "N" horizontal stripe conductor elements ~~number of said n-doped third semiconductor emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure~~.

30. (canceled)

31. (currently amended) The ESD protection structure of claim 29 ~~25~~ whereby said base horizontal conductor contact stripes ~~plurality of second semiconductor base region electrical contact conductor elements~~ and said multiple emitter elements ~~third semiconductor emitter~~

~~region electrical contact conductors~~ are ~~ultimately~~ connected together and to a second voltage source~~, typically ground~~.

32-46. (canceled)

47. (new) An integrated multiple vertical npn transistor ESD protection structure on a semiconductor substrate comprising:

a first semiconductor layer having a first conductivity type with a first dopant concentration;

a second semiconductor layer overlying said first semiconductor layer, said second semiconductor layer having said first conductivity type with a second dopant concentration;

a third semiconductor layer overlying said second semiconductor layer, said third semiconductor layer having a second conductivity type;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a first top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity type laterally spaced from said first regions, being electrically connected to said third semiconductor layer having a second top element making electrical contact to said second regions and said second semiconductor layer; and

a plurality of third regions of said first semiconductor layer conductivity type laterally spaced and interposed between said second regions,

wherein said third regions form multiple emitter elements, said multiple emitter elements being electrically connected by a conductor element with "N" horizontal stripe conductor elements connected in a contiguous comb like manner by a vertical contact conductor element at one end of said horizontal stripe conductor elements.

48. (new) The ESD protection structure of claim 47 whereby the plurality of first regions together with the associated connected first semiconductor layer are with n dopant and form multiple collector elements of a bipolar transistor array in which the base elements are formed by said third semiconductor layer and associated said plurality of second regions, said second regions having p dopant.

49. (new) The ESD protection structure of claim 48 whereby said plurality of laterally spaced third regions by which said multiple emitter elements are formed are arranged in an alternating array within said third semiconductor layer, with "N" number of emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

50. (new) The ESD protection structure of claim 49 whereby said collector elements have horizontal contact conductor stripes at the top and bottom of said transistor array which are

ultimately connected together and to a first voltage source of an input or output pin of an integrated circuit for preventing electrostatic discharge damage to said integrated circuit.

51. (new) The ESD protection structure of claim 50 whereby said base elements have horizontal conductor contact stripes, a first base horizontal conductor contact stripe positioned between the bottom horizontal collector contact stripe and said "N" horizontal stripe conductor elements and a second base horizontal conductor contact stripe positioned between the top horizontal collector contact stripe and said "N" horizontal stripe conductor elements.

52. (new) The ESD protection structure of claim 51 whereby said base horizontal conductor contact stripes and said multiple emitter elements are connected together and to a second voltage source.

53. (new) The ESD protection structure of claim 52, wherein said second voltage source is ground.